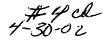


**PATENT** 





Express Mail Label No:	EL888549295US	Date of Deposit:	December 10, 2001
I hereby certify that this p service under 37 CFR Sec 20231.	aper and fee are being deposited w . 1.10 on the date indicated above	ith the United States Postal and is addressed to the Ass	Service Express Mail Post Office to Addressee istant Commissioner for Patents, Washington, D.C.
<u>Karen Orzechowski</u> Name of Person Mailing F	Paper Si <sub>l</sub>	Karen Dryg gnature of Person Mailing	chowski

### UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: J. L. Calvignac et al.

December 10, 2001

Serial No.:

unassigned

IPLaw 9CCA/B002

IBM Corporation

Filed:

(Herewith)

PO Box 12195

Res. Tri. Park, NC 27709

Title: CHIP TO CHIP INTERFACE FOR

INTERCONNECTING CHIPS

Group Art Unit:

#### **INFORMATION DISCLOSURE STATEMENT**

Assistant Commissioner for Patents Washington, D.C. 20231

Dear Sir:

This Information Disclosure Statement is being submitted in connection with the above-identified application for patent. Applicants submit herewith patents, publications or other information of which they are aware, which they believe may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 C.F.R. § 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 C.F.R. § 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(a) exists.

Docket: RAL9200001261

The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 C.F.R. § 1.98(a)(1).

A copy of each of the items identified on the attached Form PTO-1449 is supplied herewith.

Respectfully submitted,

Joscelyn G. Cockburn Attorney of Record Reg. No. 27,069

JGC:ko Enclosures

Phone: 919-543-9036 Fax: 919-254-2649

# LIST OF PATENTS AND PUBLICATIONS FOR APPLICANTS' INFORMATION DISCLOSURE STATEMENT

Serial No.:

Applicants: Jean L. Calvignac et al.

Filing Date: (herewith)

Group:

Atty. Docket No.: RAL920000126US1

#### Reference Designation

#### **U.S. PATENT DOCUMENTS**

		<del></del>				
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
AAA	5,105,424	4/14/92	Fraig et al.	370	94.1	6/2/88
ABA	5,802,055	9/1/98	Krein et al.	370	402	4/22/96
ACA	5,954,810	9/21/99	Toillon et al.	710	129	6/5/97
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AEA	6,018,782	1/25/2000	Hartmann et al.	710	129	7/14/97
AFA	6,104,696	8/15/2000	Kadambi et al.	370	218	6/30/99
AGA						
AHA						
AIA	<u></u>	<b> </b>	,	<del></del>		
AJA						
AKA				<u> </u>	-	
ALA						

#### **FOREIGN PATENT DOCUMENTS**

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
AQA						

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial	
ARA	Pending Patent Application, J. L. Calvignac et al., "High Speed Network Processor", serial number 09/838,395, filed April 19, 2001 (docket RAL920010017US2), priority date March 5, 2001.
ASA	IBM Technical Disclosure Bulletin, Vol. 38, No. 02 February 1995, "IEEE P1394 Link Level Virtual First In/First Outs for Command Block and Status Block Reception and Signaling", pages 603-606.
AST	
Examiner:	Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.